SPAD Pixel Front-End Circuit With 641 Mcps Maximum Count Rate

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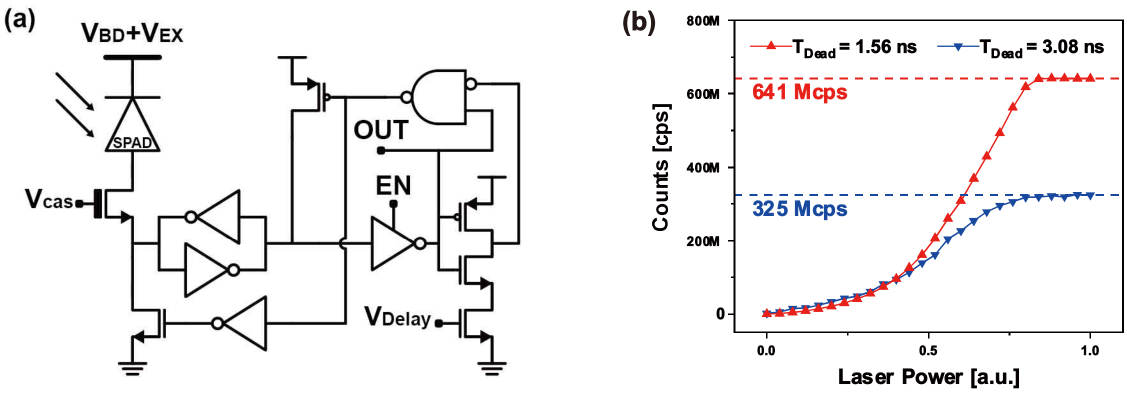

Fig. 1: (a) Schematic of the SPAD pixel front-end circuit. (b) Measurement results of the maximum count rate.

We present a single-photon avalanche diode (SPAD) pixel designed and fabricated using a 110 nm backside illumination (BSI) CMOS image sensor (CIS) process. The SPAD device utilizes a P-well/deep N-well junction structure. To maximize its performance, backside scattering technology (BST) and backside deep trench isolation (BDTI) are integrated into the device. The pixel features a circular active area with a diameter of 10 μm within a pixel pitch of 22.5 μm, resulting in a fill factor of 15.5%. At an excess bias voltage (V_{EX}) of 3 V, the device exhibits a normalized dark count rate (DCR) of 1.34 cps/μm^2. The photon detection probability (PDP) is measured to be 55% at the peak wavelength of 725 nm and 40% at 850 nm under the same bias condition.

The pixel front-end circuit, illustrated in Fig. 1(a), adopts the latch-based variable load quenching circuit (VLQC) architecture [1]. While conventional latch-based designs typically utilize high-voltage (thick-gate) transistors for the entire front-end to withstand a high excess bias voltage, such an approach limits the fill factor due to the large footprint. To address this limitation, we have introduced a thick-gate clamping transistor biased by V_{cas} into the circuit. This clamping device effectively shields the subsequent logic from the high voltage stress (up to 4 V), and consequently, the remaining components can be implemented using compact thin-gate transistors. This hybrid configuration significantly improves area efficiency compared to prior all thick-gate implementations while preserving the operational stability of the latch structure.

The circuit performance is characterized at V_{EX} = 4 V. A key feature is the variable dead time control via a current-starved inverter. The measured minimum dead time is ~1.56 ns, extracted from the inter-arrival time (IAT) histogram. As the delay voltage (V_{Delay}) is adjusted to 0.7 V, the dead time is extended to ~3.08 ns. Fig. 1(b) shows the maximum count rate (MCR) results, and at the minimum dead time, the pixel achieves an MCR of ~641 Mcps. The dynamic range is ~88 dB in single-shot mode and ~132 dB with 1-second integration. The pulse width jitter is ~20 ps under MCR conditions.

In conclusion, The proposed readout scheme effectively supports high-speed photon counting by achieving a high MCR with tunable dead time. Furthermore, future work will focus on the optimization of circuit configuration and transistor sizing. By further minimizing the front-end circuit area, we aim to reduce the pixel pitch, facilitating the development of higher-resolution SPAD arrays.

Reference

[1] S. Tisa, F. Guerrieri, and F. Zappa, "Variable-load quenching circuit for single-photon avalanche diodes," *Opt. Express*, vol. 16, no. 3, pp. 2232–2244, Feb. 2008.

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